GAU 2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Docket No.: 303.586US1
Filed: May 26, 1999
Examiner: Anh-Quan Tra

Serial No.: 09/320,421
Due Date: September 21, 2000
Group Art Unit: 2816

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response (13 Pages).

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By:
Atty: Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 21 day of September, 2000.

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Name

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Customer Number 21186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)
(GENERAL)

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Appeal
9/29/00

S/N 09/320,421 PATENT

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AMENDMENT AND RESPONSE

Commissioner for Patents
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Applicant has reviewed the Office Action mailed on June 21, 2000. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please amend claims 1-5, 10-12, 23, 25, 29, 32-40, 44-45 as follows:

Sub B1

1. (Once amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a [pair of transistors] dual-gate transistor of a second conductivity type [coupled at a drain region and coupled at a source region, and] wherein [the] a drain region for the [pair of transistors] dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a first gate of [a first one of the pair of transistors] the dual-gate transistor in each inverter; and

A1

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the [pair of transistors] dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

2. (Once amended) The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the [pair of transistors] dual-gate transistor of a second conductivity type [are] is an n-channel metal oxide semiconductor (NMOS) [transistors] transistor.